(b) Name various secondary effects in the operation of MOSFET.

(c) Why substrate is normally shorted with source in MOSFET ?

(d) Why scaling of the MOS devices is carried out ?

(e) What is noise margin ?

(f) What are the advantages of CMOS circuits over BJT circuits ?

(g) What is specified using the word technology ?

(h) Name various reliability issues in CMOS design.

(i) What do you mean by channel length modulation ?

(j) What is the meaning of rise time of CMOS logic circuits ? **1.5×10=15**

Roll No. ..... **Total Pages : 04**

J-21-0151

B. Tech. EXAMINATION, 2021

Semester VII (CBCS)

VLSI DESIGN

EC-704

Time : 2 Hours *Maximum Marks : 60*

The candidates shall limit their answers precisely within 20 pages only (A4 size sheets/assignment sheets), no extra sheet allowed. The candidates should write only on one side of the page and the back side of the page should remain blank. Only blue ball pen is admissible.

Note : Attempt *Four* questions in all, selecting *one* question from any of the Sections A, B, C and D. Q. No. **9** is compulsory.

Section A

1. (a) Differentiate between depletion mode MOSFET and enhancement type MOSFET. Explain the working of enhancement mode NMOSFET in linear and saturation region with clear sketches. **8**

(b) Explain VLSI circuit design flow. 7

2. (a) Derive the I-V characteristics of MOSFET in all the mode of operation. 8

(b) What is threshold voltage ? What are the different factors on which it depends ? 7

Section B

3. (a) With the neat sketches explain the complete process flow for CMOS circuit. 8

(b) Explain the working of CMOS inverter. What are the advantages of using CMOS inverter over simple NMOS inverter ? 7

4. (a) What are the dynamic logic circuits ? Enumerate various differences between dynamic and static logic circuits. Explain the limitations of dynamic logic circuits. 8

(b) What are the different causes of power dissipation in CMOS circuits ? Explain each in detail with necessary expressions. 7

Section C

5. (a) Implement the logic circuit using CMOS configuration for F = A + (B.C) and draw its stick diagram. 8

(b) Discuss the various aspects of designing a simple SRAM using the CMOS circuit configuration. 7

6. (a) Draw 2 input NOR and NAND gate. Also make stick diagram for each. 8

(b) Explain, how a layout designing is different from stick diagram designing. Explain lambda based design rules for the layout designing. 7

Section D

7. (a) What is single stage common source amplifier ? Derive the expression for its voltage gain. 8

(b) Derive the expression for output impedance of the CMOS differential amplifier. 7

8. (a) Discuss the design requirements for a simple CMOS differential high gain amplifier. 8

(b) Explain the characteristics of common gate amplifier. 7

(Compulsory Question)

9. (a) What do you mean by weak inversion condition ?